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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

QUICKLOGIC CORPORATION,

Plaintiff,

v.

KONDA TECHNOLOGIES, INC., AND VENKAT KONDA,

Defendants.

Case No. 5:21-cv-4657

COMPLAINT FOR DECLARATORY JUDGMENT OF NONINFRINGEMENT AND NON-BREACH OF CONTRACT

DEMAND FOR JURY TRIAL

Plaintiff QuickLogic Corporation ("QuickLogic") seeks a declaratory judgment that it has not breached any contractual commitment or infringed on any claim of patents as asserted by Konda Technologies, Inc. through the actions of its CEO, Venkat Konda (collectively, "Defendants").

There is a live and existing controversy between the parties to this lawsuit. Between April and May, 2021, Defendants sent a series of communications to QuickLogic alleging that QuickLogic infringed patents identified in the Konda Technologies FPGA Interconnect Patent Portfolio ("Patent Portfolio", Exhibit 2)[1] and breached a 2010 Consulting and License Agreement between the parties ("the 2010 Agreement", Exhibit 3).

After several communications, Defendants sent a cease and desist letter alleging unauthorized use of the Patent Portfolio and violation of the 2010 Agreement. (Exhibit 5.) For its part, QuickLogic repeatedly offered to discuss Defendants' allegations to seek informal resolution. (Exhibit 6.) Defendants did not engage with QuickLogic to resolve the matter and continued to assert, without explanation, particularity or specificity, that QuickLogic was improperly using Defendants' patents and violating the 2010 Agreement. Thus, QuickLogic seeks a declaration from this Court that its activities are not infringing the Asserted Patents or violating the 2010 Agreement.

INTRODUCTION

1. This is an action for a declaratory judgment arising under the patent laws of the United States, Title 35 of the United States Code. QuickLogic seeks a declaratory judgment that it does not infringe any claim of the Asserted Patents. The action arises from a real and immediate controversy between the QuickLogic and the Defendants as to whether QuickLogic infringes any claims of the Asserted Patents.

2. On April 30, 2021 the Defendants emailed the CEO of QuickLogic inquiring whether QuickLogic was violating the 2010 Agreement through its involvement with an open source initiative. (Exhibit 1.) The CEO of QuickLogic replied that because QuickLogic "did not commercialize" the Defendants' "architecture," QuickLogic did not violate the 2010 Agreement

[1] The 2010 Agreement licensed to QuickLogic certain patent rights and Defendants' recent assertions do not challenge that QuickLogic is licensed to use those rights. As described later in this Complaint, the patents at issue in this case are the "Asserted Patents."

and thus did not infringe the Patent Portfolio. (Exhibit 1.) Defendants proceeded to send additional emails asking for response to their assertion that QuickLogic did use the Patent Portfolio. (Exhibit 1.) After back and forth communication, Defendants sent a cease and desist letter alleging (1) unauthorized use of the Patent Portfolio and (2) violation of the 2010 Agreement. (Exhibit 5.) The letter concludes with an explicit statement that "this letter serves as a pre-suit notice for a lawsuit against you." (Exhibit 5.) Therefore, because of the Defendants' threat of suit, QuickLogic believes there is an immediate, substantial, and judiciable controversy whether its programmable logic products infringe the Asserted Patents and whether it has breached the 2010 Agreement.

3. The threat of an imminent lawsuit is bolstered by Defendants' history of bringing suits on similar grounds. Defendants' website demonstrates their strong emphasis and focus on its multiple past and present suits against alleged patent infringers. (Exhibit 7.) Eight out of fifteen substantive pages of the website are devoted to narrative updates of the suits brought against alleged "fraudsters." (Exhibit 7.) Because of the Defendants' track record, it is very likely the threat of suit in the cease and desist letter is very real. Therefore, a declaratory judgment of patent noninfringement would resolve a real and very immediate controversy.

4. The Defendants' actions have created a real and immediate controversy between the Defendants and QuickLogic as to whether their products and/or services infringe any claims of the Asserted Patents and as to whether QuickLogic has breached the 2010 Agreement. The facts and allegations recited herein show that there is a real, immediate, and justiciable controversy concerning these issues.

THE PARTIES

5. QuickLogic Corporation is a Delaware corporation with a place of business at 2220 Lundy Ave., San Jose, California 95131.

6. On information and belief, Konda Technologies, Inc. is a company incorporated and registered under the laws of California with a principal place of business in San Jose, California. Konda Technologies holds itself out as an intellectual property licensing company, a non-practicing entity.

7. On information and belief, Venkat Konda is an individual who resides in Santa

Clara County, California. On information and belief, Venkat Konda is the CEO of Konda Technologies, Inc.

JURISDICTIONAL STATEMENT

8. This action arises under the Declaratory Judgment Act, 28 U.S.C. § 2201 et seq., and under the patent laws of the United States, Title 35 of the United States Code.

9. This Court has subject matter jurisdiction over the claims alleged in this action under 28 U.S.C. §§ 1331, 1338, 1367, 2201, and 2202 because this Court has exclusive jurisdiction over declaratory judgment claims arising under the patent laws of the United States pursuant to 28 U.S.C. §§ 1331, 1338, 2201, and 2202. This Court also has supplemental jurisdiction over the declaratory judgment claim of non-breach of the 2010 Agreement under 28 U.S.C. § 1367 because it is related to the patent noninfringement claims such that they form part of the same case or controversy to which this court has exclusive jurisdiction over pursuant to 28 U.S.C. §§ 1331, 1338, 1367, 2201, and 2202.

10. This Court can provide the declaratory relief sought in this Complaint because an actual case and controversy exists between the parties within the scope of this Court's jurisdiction pursuant to 28 U.S.C. § 2201. As described in this Complaint, an actual case and controversy exists at least because Defendants' have asserted that QuickLogic infringes the Patent Portfolio and has breached the 2010 Agreement. Further, Defendants specified in a cease and desist letter that the letter served "as a pre-suit notice for a lawsuit" and that the Defendants "will have no choice but to pursue all legal causes of action" if the Plaintiffs did not comply with the letter's demands. (Exhibit 5.)

11. This Court has personal jurisdiction over the Defendants because the Defendants have engaged in actions in this District that form the basis of the Plaintiff's claims against the Defendants. First, Konda Technologies, Inc. is incorporated in the state and has its primary place of business in the District. Therefore, Konda Technologies, Inc. is subject to general personal jurisdiction. Second, the Defendants have entered into several contracts with QuickLogic in the District. Third, the Defendants have availed themselves of the District by bringing suit against another company, alleging infringement of the U.S. Patent No. 10,003,553. (*See, e.g.*, Case No.

5:18-cv-07581-LHK.) Fourth, alleging unauthorized use of the Patent Portfolio and violation of the 2010 Agreement entered into within the District, the Defendants have sent an email cease and desist letter, which the Defendants characterized as pre-suit notice for a lawsuit.

12. Therefore, the Defendants have availed themselves of the District and have created a real, live, immediate, and justiciable case or controversy between the Defendants and the Plaintiff.

13. In doing so, the Defendants have established sufficient minimum contacts with the Northern District of California such that the Defendants are subject to specific personal jurisdiction in this action. Further, the exercise of personal jurisdiction based on these repeated and pertinent contacts does not offend traditional notions of fairness and substantial justice.

14. Venue is proper in this District under 28 U.S.C. §§ 1391 and 1400, including because, under Ninth and Federal Circuit law, venue in declaratory judgment actions for noninfringement of patents is determined under the general venue statute, 28 U.S.C. § 1391.

15. Under 28 U.S.C. § 1391(b)(1), venue is proper in any judicial district where a defendant resides, if all defendants are residents of the State in which the district is located. Entities with the capacity to sue and be sued, such as the Defendants, are deemed to reside, if defendants, in any judicial district in which such defendants are subject to the court's personal jurisdiction with respect to the civil action in question under 28 U.S.C. § 1391(c).

16. As discussed above, on information and belief Defendant Konda is domiciled within the Northern District of California and is therefore deemed to reside within this District under 28 U.S.C. § 1391. Moreover, the Defendants are subject to personal jurisdiction with respect to this action in the Northern District of California, and thus, at least for the purposes of this action, the Defendants reside in the Northern District of California and venue is proper under 28 U.S.C. § 1391.

17. Venue is also proper in this judicial district under 28 U.S.C. § 1400(b) because Defendants are located in this judicial district and Konda Technologies, Inc. is incorporated in California. Venue is also proper because the alleged acts giving rise to the infringement allegations all took place in this District.

FACTUAL BACKGROUND

18. Between April and May, 2021, Defendants sent a series of communications to QuickLogic ultimately culminating in a cease and desist letter from Defendants alleging unauthorized use of the Patent Portfolio and violation of the 2010 Agreement. On April 30, 2021, Defendants emailed Brian Faith, CEO of QuickLogic, concerning QuickLogic's involvement with open source initiatives and its compliance with the 2010 Agreement. (Exhibit 1.) The open source initiatives are limited to joining the Open Source FPGA Foundation as a founding and Premier Member, and the QuickLogic Open Reconfigurable Computing Initiative. (Exhibit 1.) Faith confirmed the pursuit of the open source initiatives were in compliance with the 2010 Agreement. (Exhibit 1.) Despite the confirmation, Defendants sent a cease and desist alleging (1) unauthorized use of the Patent Portfolio and (2) violation of the 2010 Agreement. (Exhibit 5.) Notably, the letter did not provide explanation to support the conclusory statements. (Exhibit 5.) The letter concludes with an explicit statement that "this letter serves as a pre-suit notice for a lawsuit against you." (Exhibit 5.)

19. As apparently conceded in Defendants' demands, QuickLogic is licensed to certain patent rights in the Patent Portfolio pursuant to the 2010 Agreement. Therefore, only the *unlicensed patents* in the Patent Portfolio are at issue in this case. Specifically, U.S. Patent Nos. 9,374,322 (the "'322 Patent", Exhibit 8), 9,509,634 (the "'634 Patent", Exhibit 9), 9,929,977 (the "'977 Patent", Exhibit 10), 10,536,399 (the "'399 Patent", Exhibit 11), 10,412,025 (the "'025 Patent", Exhibit 12) 10,574,594 (the "'594 Patent", Exhibit 13), 10,992,597 (the "'597 Patent", Exhibit 14), 10,965,618 (the "'618 Patent", Exhibit 15), and 10,979,366 (the "'366 Patent", Exhibit 16) (collectively, the "Asserted Patents").[2] As to the remainder of the patent rights contained in the Patent Portfolio, the 2010 Agreement provides a license to use them. Specifically, Section 1.2 of the 2010 Agreement states:

> "Konda hereby grants to QuickLogic a non-exclusive, royalty-free, irrevocable and world-wide right, with rights to sublicense through multiple tiers of sublicensees, to

[2] U.S. Patent No. 10,003,533 is also a part of the Patent Portfolio, but as described below, it was invalidated by the PTAB so it is not at issue in this case.

> reproduce, make derivative works of, publicly perform, publicly display and distribute in any form or medium . . . and to make, have made, use, import, offer to sell, and sell the Konda Intellectual Property incorporated or used in the programmable logic of QuickLogic products or used in . . . commercializing QuickLogic's technology."

(Exhibit 3 at 1.)

20. Pursuant to Section 8.7 of the 2010 Agreement, QuickLogic attempted to engage in Informal Dispute Resolution between May 26, 2021 and June 16, 2021 to resolve the differences in opinion regarding the parties' obligations under the 2010 Agreement. Ex. 17. Section 8.7 affords the parties 10 business days, starting from QuickLogic's May 26, 2021 letter, to resolve any disputes. Ex. 3 at 5; Ex. 6. QuickLogic unilaterally extended this period another week, to June 16, 2021, in a good faith effort to resolve the parties' disagreements. During this time, despite correspondence from Defendants on other matters, Defendants repeatedly ignored requests from QuickLogic to provide support for Defendants' claims of alleged infringement and violation of the 2010 Agreement. *See* Ex. 17 at 2-3 (requesting support for positions on June 15, 2021); *id.* at 6 (same on June 10, 2021), *id.* at 9 (same on June 9, 2021) (citing Ex. 6). Without explanation, Defendants also refused to participate in a videoconference with officers of QuickLogic scheduled for June 16, 2021. Defendants' inability or unwillingness to even provide a basis for their allegations doomed any meaningful, good faith Informal Dispute Resolution. Defendants' conduct accordingly necessitated this action.

21. One of the patents recently asserted in the Patent Portfolio is U.S. Patent No. 10,003,553 (the "'553 Patent"). The '553 Patent was invalidated by the Patent Trial and Appeal Board (PTAB) on multiple grounds in March 2021. *See Flex Logix Techologies Inc. v. Konda,* No. PGR2019-00037 (P.T.A.B. March 16, 2021). The PTAB held all claims of the '553 Patent failed to meet the (1) definiteness requirement under 35 U.S.C. § 112(b), (2) written description requirement under 35 U.S.C. § 112(a), and (3) enablement requirement under 35 U.S.C. § 112(a). *Id.* at 16, 19, 21. Despite this invalidity finding, the Defendants assert that QuickLogic infringes the '553 Patent.

22. QuickLogic understands that Defendants are accusing the following products of infringing: (1) EOS S3 family of devices; (2) PolarPro 3/3E family of devices; (3) eFPGA IP cores based on the same FPGA architecture as in (1) and (2); and (4) the associated Open Source FPGA Software Tools that support them.

INTRADISTRICT ASSIGNMENT

23. For purposes of intradistrict assignment under Civil Local Rules 3-2(c) and 3-5(b), this Intellectual Property Action will be assigned on a district-wide basis. QuickLogic requests that the case be assigned to the San Jose Division because both the Plaintiff and Defendants have their primary places of business and residence in Santa Clara County. (Exhibits 3 and 5.) In particular, QuickLogic requests that the case should be assigned to the Honorable Lucy H. Koh, who presided over Konda Technologies, Inc.'s prior lawsuit against another company alleging infringement of the '533 Patent. (*See, e.g.*, Case No. 5:18-cv-07581-LHK.)

FIRST CLAIM FOR RELIEF

(Declaratory Judgment That QuickLogic Does Not Infringe The '322 Patent)

24. QuickLogic repeats and realleges each and every allegation contained in paragraphs 1 through 23 of this Complaint as if fully set forth herein.

25. In view of the facts and allegations set forth above, there is an actual, justiciable, substantial, and immediate controversy between QuickLogic and Defendants regarding infringement of the '322 Patent.

26. QuickLogic seeks a declaration that it does not infringe, and has not infringed, any claim of the '322 Patent.

27. The '322 Patent is titled "Optimization of multi-stage hierarchical networks for practical routing applications" and purports to "significantly optimized multi-stage networks, useful in wide target applications, with VLSI layouts using only horizontal and vertical links to route large scale sub-integrated circuit blocks having inlet and outlet links, and laid out in an integrated circuit device in a two-dimensional grid arrangement of blocks are presented. The optimized multi-stage networks in each block employ several rings of stages of switches with inlet and outlet links of sub-integrated circuit blocks connecting to rings from either left-hand side only,

or from right-hand side only, or from both left-hand side and right-hand side; and employ shuffle exchange links where outlet links of cross links from switches in a stage of a ring in one sub-integrated circuit block are connected to either inlet links of switches in the another stage of a ring in the same or another sub-integrated circuit block." (Exhibit 8.)

28. Although Defendants have not called out any particular claims as being infringed, Claim 1 of the '322 Patent is exemplary:

> 1. A programmable integrated circuit comprising a plurality of programmable logic blocks and a network, and
>
> said each plurality of programmable logic blocks comprising a plurality of inlet links and a plurality of outlet links; and
>
> said network further comprising a plurality of subnetworks, with each said subnetwork coupled with one of said plurality of programmable logic blocks; and
>
> said plurality of subnetworks coupled with said plurality of programmable logic blocks arranged in a two-dimensional grid of rows and columns; and
>
> said each subnetwork comprising r rings, and said each ring comprising y_r stages, where $r \geqq 1$; $y_r \geqq 1$; and
>
> Said each stage comprising a switch of size $d_i \times d_o$, where $d_i \geqq 2$ and $d_o \geqq 2$ and each said switch of size $d_i \times d_o$ having di incoming links and do outgoing links; and
>
> said each switch comprising a plurality of multiplexers, and said each multiplexer is of size p:1 where p>1; and
>
> Said outlet links are connecting to one or more of the said incoming links of any said switch of any stage of any ring of said coupled subnetwork, and said inlet links are connecting from one of said outgoing links of any said switch of any stage of any ring of said coupled subnetwork; and
>
> Said incoming links and outgoing links in each said switch in said each stage of said each subnetwork comprising a plurality of forward connecting links

connecting from switches in lower stage to switches in the immediate succeeding higher stage in the same ring, and also comprising a plurality of backward connecting links connecting from switches in higher stage to switches in the immediate preceding lower stage in the same ring; and

Said forward connecting links comprising a plurality of straight links connecting from a switch in a stage of a ring in a subnetwork to a switch in another stage of the same ring in the same subnetwork and also comprising a plurality of cross links connecting from a switch in a stage of a ring in a subnetwork to a switch in another stage of another ring in the same subnetwork or to a switch in another stage of another ring in a different subnetwork, and

Said backward connecting links comprising a plurality of straight links connecting from a switch in a stage of a ring in a subnetwork to a switch in another stage of the same ring in the same subnetwork and also comprising a plurality of cross links connecting from a switch in a stage of a ring in a subnetwork to a switch in another stage of another ring the same subnetwork or to a switch in another stage of another ring in a different subnetwork, and

Said plurality of multiplexers in one or more said stages are connected so that said one or more forward connecting links are fed back into said one or more backward connecting links through one or more said multiplexers, and also said plurality of multiplexers in one or more said stages are connected so that one or more said backward connecting links are fed back into one or more said forward connecting links through one or more said multiplexers; and

Said cross links between switches of stages of rings between any two different subnetworks are connecting as either vertical links only, or horizontal links only, or both vertical links and horizontal links.

(Exhibit 8.)

29. QuickLogic does not infringe Claim 1 or any other claims of the '322 Patent and seeks such a declaration to resolve the actual dispute between the parties.

SECOND CLAIM FOR RELIEF

(Declaratory Judgment That QuickLogic Does Not Infringe The '634 Patent)

30. QuickLogic repeats and realleges each and every allegation contained in paragraphs 1 through 29 of this Complaint as if fully set forth herein.

31. In view of the facts and allegations set forth above, there is an actual, justiciable, substantial, and immediate controversy between QuickLogic and Defendants regarding infringement of the '634 Patent.

32. QuickLogic seeks a declaration that it does not infringe, and has not infringed, any claim of the '634 Patent.

33. The '634 Patent is titled "Fast scheduling and optimization of multi-stage hierarchical networks" and purports to "Significantly optimized multi-stage networks with scheduling methods for faster scheduling of connections, useful in wide target applications, with VLSI layouts using only horizontal and vertical links to route large scale sub-integrated circuit blocks having inlet and outlet links, and laid out in an integrated circuit device in a two-dimensional grid arrangement of blocks are presented. The optimized multi-stage networks in each block employ several slices of rings of stages of switches with inlet and outlet links of sub-integrated circuit blocks connecting to rings from either left-hand side only, or from right-hand side only, or from both left-hand side and right-hand side; and employ multi-drop links where outlet links of cross links from switches in a stage of a ring in one sub-integrated circuit block are connected to either inlet links of switches in the another stage of a ring in the same or another sub-integrated circuit block." (Exhibit 9.)

34. Although Defendants have not called out any particular claims as being infringed, Claim 1 of the '634 Patent is exemplary:

> 1. A programmable integrated circuit comprising a plurality of programmable logic blocks and a network, and

said each plurality of programmable logic blocks comprising a plurality of inlet links and a plurality of outlet links; and

said network further comprising a plurality of subnetworks, with each said subnetwork coupled with one of said plurality of programmable logic blocks; and

said plurality of subnetworks coupled with said plurality of programmable logic blocks arranged in a two-dimensional grid of rows and columns; and

said each subnetwork comprising r rings, and said each ring comprising y_r stages, where $r \geqq 1$; $y_r \geqq 1$; and

Said each stage comprising a switch of size $d_i \times d_0$, where $d_i \geqq 2$ and $d_o \geqq 2$ and each said switch of size $d_i \times d_0$ having d_i incoming links and d_0 outgoing links; and

said each switch comprising a plurality of multiplexers, and said each multiplexer is of size p:1 where p>1; and

Said outlet links are connecting to one or more of the said incoming links of any said switch of any stage of any ring of said coupled subnetwork, and said inlet links are connecting from one of said outgoing links of any said switch of any stage of any ring of said coupled subnetwork; and

Said incoming links and outgoing links in each said switch in said each stage of said each subnetwork comprising a plurality of forward connecting links connecting from switches in lower stage to switches in the immediate succeeding higher stage in the same ring, and also comprising a plurality of backward connecting links connecting from switches in higher stage to switches in the immediate preceding lower stage in the same ring; and

Said forward connecting links comprising a plurality of straight links connecting from a switch in a stage of a ring in a subnetwork to a switch in another stage of the same ring in the same subnetwork and also comprising a plurality of cross links connecting from a switch in a stage of a ring in a

subnetwork to a switch in another stage of another ring in the same subnetwork or to a switch in another stage of another ring in a different subnetwork, and

Said backward connecting links comprising a plurality of straight links connecting from a switch in a stage of a ring in a subnetwork to a switch in another stage of the same ring in the same subnetwork and also comprising a plurality of cross links connecting from a switch in a stage of a ring in a subnetwork to a switch in another stage of another ring the same subnetwork or to a switch in another stage of another ring in a different subnetwork, and

Said plurality of multiplexers in one or more said stages are connected so that said one or more forward connecting links are fed back into said one or more backward connecting links through one or more said multiplexers, and also said plurality of multiplexers in one or more said stages are connected so that one or more said backward connecting links are fed back into one or more said forward connecting links through one or more said multiplexers; and

Said cross links between switches of stages of rings between any two different subnetworks are connecting as either vertical links only, or horizontal links only, or both vertical links and horizontal links;

Said each subnetwork further partitioned into a plurality of slices so that there is zero or more connections from one said slice to another said slice with in each said subnetwork; said no two slices further having any common outlet links connecting from said coupled programmable logic block; said cross links are connecting from a said slice of any said subnetwork to a corresponding said slice of any other said subnetwork; said some slices of said each subnetwork comprising paths only to inlet links of said couple programmable logic block and said some other slices of said each

subnetwork comprising paths only to said slices of said another subnetwork.

(Exhibit 9.)

35. QuickLogic does not infringe Claim 1 or any other claims of the '634 Patent and seeks such a declaration to resolve the actual dispute between the parties.

THIRD CLAIM FOR RELIEF

(Declaratory Judgment That QuickLogic Does Not Infringe The '977 Patent)

36. QuickLogic repeats and realleges each and every allegation contained in paragraphs 1 through 35 of this Complaint as if fully set forth herein.

37. In view of the facts and allegations set forth above, there is an actual, justiciable, substantial, and immediate controversy between QuickLogic and Defendants regarding infringement of the '977 Patent.

38. QuickLogic seeks a declaration that it does not infringe, and has not infringed, any claim of the '977 Patent.

39. The '977 Patent is titled "Fast scheduling and optimization of multi-stage hierarchical networks" and purports to "Significantly optimized multi-stage networks with scheduling methods for faster scheduling of connections, useful in wide target applications, with VLSI layouts using only horizontal and vertical links to route large scale sub-integrated circuit blocks having inlet and outlet links, and laid out in an integrated circuit device in a two-dimensional grid arrangement of blocks are presented. The optimized multi-stage networks in each block employ several slices of rings of stages of switches with inlet and outlet links of sub-integrated circuit blocks connecting to rings from either left-hand side only, or from right-hand side only, or from both left-hand side and right-hand side; and employ multi-drop links where outlet links of cross links from switches in a stage of a ring in one sub-integrated circuit block are connected to either inlet links of switches in the another stage of a ring in the same or another sub-integrated circuit block." (Exhibit 10.)

40. Although Defendants have not called out any particular claims as being infringed, Claim 1 of the '977 Patent is exemplary:

1. A network comprising a plurality of subnetworks, Said plurality of

subnetworks comprising a plurality of inlet links and a plurality of outlet links, and said plurality of subnetworks arranged in a two-dimensional grid of rows and columns; and

each subnetwork comprising r rings, and each ring comprising y_r stages, where $r \geq 1$; $y_r \geq 1$; and

each stage comprising a switch of size $d_i \times d_0$, where $d_i \geq 2$ and $d_o \geq 2$ and each switch of size $d_i \times d_0$ having d_i incoming links and d_0 outgoing links; and

each switch comprising a plurality of multiplexers, and each multiplexer is of size p:1 where p>1; and

Said inlet links are connected to one or more of said incoming links of a said switch of a stage of a ring of said subnetwork, and said outlet links are connected to one of said outgoing links of a said switch of a stage of a ring of said subnetwork; and

each subnetwork of the plurality of subnetworks may not be comprising the same number of said inlet links and may not be comprising the same number of said out links; each subnetwork of the plurality of subnetworks may not be comprising the same number of said rings, each ring may not be comprising the same number of said stages; each stage may not be comprising the same number of switches; and each switch in each stage may not be of the same size, each multiplexer in each stage may not be of the same size and

Said incoming links and outgoing links in each switch in each stage of each ring of each subnetwork comprising a plurality of forward connecting links connected from switches in a stage to switches in another stage in same said ring or another said ring, and also comprising a plurality of backward connecting links connected from switches in a stage to switches in another stage in same ring or another said ring; and

Said forward connecting links comprising zero or more straight links connected

from a switch in a stage of a ring in a subnetwork to a switch in another stage of the same ring in the same subnetwork and also comprising zero or more cross links connected from a switch in a stage of a ring in a subnetwork to a switch in the same numbered stage of another ring in the same subnetwork or to a switch in the same numbered stage of another ring in a different subnetwork, and

Said backward connecting links comprising zero or more straight links connected from a switch in a stage of a ring in a subnetwork to a switch in another stage of the same ring in the same subnetwork and also comprising zero or more cross links connected from a switch in a stage of a ring in a subnetwork to a switch in the same numbered stage of another ring the same subnetwork or to a switch in the same numbered stage of another ring in a different subnetwork, and

Said plurality of multiplexers in zero or more said stages are connected so that said zero or more forward connecting links are fed back into said zero or more backward connecting links through zero or more said multiplexers, or also said plurality of multiplexers in zero or more said stages are connected so that zero or more said backward connecting links are fed back into zero or more said forward connecting links through zero or more said multiplexers; and

Said cross links between switches of stages of rings between two said different subnetworks are connected as either vertical links only, or horizontal links only, or both vertical links and horizontal links; and

Either subnetwork further partitioned into one or more slices so that there is zero or more connections from one said slice to another said slice with in each subnetwork; or said no two slices further having common outlet links; or said cross links are connected from a said slice of a said subnetwork to a corresponding said slice of another said subnetwork; or said one or more

slices of each subnetwork comprising connections only to inlet links; or said one or more slices of each subnetwork comprising connections only to said slices of said another subnetwork.

(Exhibit 10.)

41. QuickLogic does not infringe Claim 1 or any other claims of the '977 Patent and seeks such a declaration to resolve the actual dispute between the parties.

FOURTH CLAIM FOR RELIEF

(Declaratory Judgment That QuickLogic Does Not Infringe The '399 Patent)

42. QuickLogic repeats and realleges each and every allegation contained in paragraphs 1 through 41 of this Complaint as if fully set forth herein.

43. In view of the facts and allegations set forth above, there is an actual, justiciable, substantial, and immediate controversy between QuickLogic and Defendants regarding infringement of the '399 Patent.

44. QuickLogic seeks a declaration that it does not infringe, and has not infringed, any claim of the '399 Patent.

45. The '399 Patent is titled "Automatic multi-stage fabric generation for FPGAs" and purports to "Systems and methods to automatically or manually generate various multi-stage pyramid network based fabrics, either partially connected or fully connected, are disclosed by changing different parameters of multi-stage pyramid network including such as number of slices, number of rings, number of stages, number of switches, number of multiplexers, the size of the multiplexers in any switch, connections between stages of rings either between the same numbered stages (same level stages) or different numbered stages, single or multi-drop hop wires, hop wires of different hop lengths, hop wires outgoing to different directions, hop wires incoming from different directions, number of hop wires based on the number and type of inlet and outlet links of large scale sub-integrated circuit blocks. One or more parameters are changed in each iteration so that optimized fabrics are generated, at the end of iterations, to route a given set of benchmarks or designs having a specific connection requirements." (Exhibit 11.)

46. Although Defendants have not called out any particular claims as being infringed,

Claim 1 of the '399 Patent is exemplary:

> 1. A system for generating a multi-stage pyramid based network,
>
> said multi-stage pyramid based network including connections to a plurality of programmable logic blocks of a programmable integrated circuit arranged in a two-dimensional grid of a plurality of rows and a plurality of columns,
>
> said plurality of programmable logic blocks comprising a plurality of inlet links and a plurality of outlet links; and
>
> said multi-stage pyramid based network further comprising a plurality of partial multi-stage pyramid networks wherein each programmable logic block of said plurality of programmable logic blocks coupled to at least one of said plurality of partial multi-stage pyramid networks via said plurality of inlet links and said plurality of outlet links; and
>
> each partial multi-stage pyramid network of said plurality of partial multi-stage pyramid networks further comprising one or more slices, each slice of said one or more slices further comprising one or more rings, each ring of said one or more rings further comprising a plurality of stages; and
>
> each stage of said plurality of stages comprising one or more switches of size $d_i \times d_0$, where d_i, d_o are integers, $d_i \geq 2$ and $d_o \geq 2$ and each switch of said one or more switches of size $d_i \times d_0$ having di incoming links and d_0 outgoing links; and each switch of said one or more switches of size $d_i \times d_0$ further comprising a plurality of multiplexers of size $d \geq 2$, where d is an integer, with each multiplexer of said plurality of multiplexers comprising d inputs and one output; and
>
> said one or more switches of size $d_i \times d_0$ comprises either only a forward switch, or only a backward switch, or both a forward switch and a backward switch, or a forward switch, a backward switch and a U-turn switch, or a forward switch, a backward switch and a U-turn switch without 180 degree turn paths or a forward switch, a backward switch, a U-turn switch and a reverse

U-turn switch or a forward switch, a backward switch, a U-turn switch and a reverse U-turn switch without 180 degree turn paths, or an integrated switch of a forward switch, a backward switch and a U-turn switch, or an integrated switch of a forward switch, a backward switch and a U-turn switch without 180 degree turn paths or an integrated switch of a forward switch, a backward switch, a U-turn switch and a reverse U-turn switch or an integrated switch of a forward switch, a backward switch, a U-turn switch and a reverse U-turn switch without 180 degree turn paths; and

said di incoming links and said do outgoing links comprises a plurality of internal connections and a plurality of hop wires; and

each inlet link of said plurality of inlet links is connected to the output of one multiplexer of said plurality of multiplexers of one switch of said one or more switches of one stage of said plurality of stages of one ring of said one or more rings of one slice of said one or more slices of one partial multi-stage pyramid network of said plurality of partial multi-stage pyramid networks, and each outlet link of said plurality of outlet links is connected to an input of said d inputs of one or more multiplexers of said plurality of multiplexers of one or more switches of said one or more switches of one or more stages of said plurality of stages of one or more rings of said one or more rings of one or more slices of said one or more slices of one or more partial multi-stage pyramid networks of said plurality of partial multi-stage pyramid networks; and

a first programmable logic block of said plurality of programmable logic blocks comprising the same or different number of said plurality of inlet links as a second programmable logic block of said plurality of programmable logic blocks; a first programmable logic block of said plurality of programmable logic blocks comprising the same or different number of said plurality of outlet links as a second programmable logic block of said plurality of

programmable logic blocks; a first slice of said one or more slices comprising the same or different number of said rings as a second slice of said one or more slices; a first ring of said one or more rings comprising the same or different number of said stages as a second ring of said one or more rings; a first stage of said plurality of stages comprising the same or different number of said switches as a second stage of said plurality of stages; a first switch in said one or more switches is the same or different size as a second switch in said one or more switches; a first multiplexer in said plurality of multiplexers is the same or different size as a second multiplexer in said plurality of multiplexers; and

each internal connection of said plurality of internal connections connected from the output of a first multiplexer of said plurality of multiplexers of a first switch of said one or more switches of a first stage of said plurality of stages of a first ring of said one or more rings to one of the d inputs of a second multiplexer of said plurality of multiplexers of a second switch of said one or more switches of a second stage of said plurality of stages of said first ring of said one or more rings; and

said plurality of hop wires further comprises a plurality of internal hop wires and a plurality of external hop wires; and

each internal hop wire of said plurality of internal hop wires connected from the output of a first multiplexer of said plurality of multiplexers of a first switch of said one or more switches of a first stage of said plurality of stages of a first ring of said one or more rings of a first slice of said one or more slices of a first partial multi-stage pyramid network of said plurality of partial multi-stage pyramid networks to one or more of the d inputs of one or more different multiplexers from said first multiplexer of said plurality of multiplexers of one or more different switches from said first switch of said one or more switches of one or more different stages from said first stage of

said plurality of stages of one or more different rings from said first ring of said one or more rings of said first slice of said one or more slices of said first partial multi-stage pyramid network of said plurality of partial multi-stage pyramid networks; and

each external hop wire of said plurality of external hop wires connected from the output of a multiplexer of said plurality of multiplexers of a switch of said one or more switches of a stage of said plurality of stages of a ring of said one or more rings of a slice of said one or more slices of a first said partial multi-stage pyramid network of said plurality of partial multi-stage pyramid networks to one or more inputs of said d inputs of one or more multiplexers of said plurality of multiplexers of one or more switches of said one or more switches of said plurality of stages of one or more stages of said one or more rings of a slice of said one or more slices of one or more partial multi-stage pyramid networks different from first said partial multi-stage pyramid network of said plurality of partial multi-stage pyramid networks; and

one or more external hop wires of said plurality of external hop wires are either connected between multiplexers of said plurality of multiplexers of switches of said one or more switches of same numbered stages of said plurality of stages in two or more different partial multi-stage pyramid networks of said plurality of partial multi-stage pyramid networks or connected between multiplexers of said plurality of multiplexers of switches of said one or more switches of in different numbered stages said plurality of stages in two or more different partial multi-stage pyramid networks of said plurality of partial multi-stage pyramid networks,

said system comprising:

one or more processors;

a memory arrangement coupled to said one or more processors, the memory arrangement configured with instructions that when executed by said one or

more processors cause said one or more processors to perform operations including:

setting up size of said one or more slices, setting up size of said one or more rings, setting up size of said plurality of stages, setting up size of said one or more switches, setting up size of said plurality of multiplexers, setting up number of inputs of each multiplexer of said plurality of multiplexers;

setting up connections of said plurality of inlet links and said plurality of outlet links to said plurality of partial multi-stage pyramid networks;

setting up connections of said plurality of internal connections between said plurality of stages of the same ring of said one or more rings;

selecting hop length of each external hop wire of said plurality of external hop wires, setting up connections of said plurality of external hop wires between said plurality of partial multi-stage pyramid networks;

setting up connections of said plurality of internal hop wires between said one or more rings of the same slice of said one or more slices of a partial multi-stage pyramid network of said plurality of partial multi-stage pyramid networks;

setting up size of said plurality of rows and size of said plurality of columns in said two-dimensional grid;

simulating said programmable integrated circuit with said plurality of rows and said plurality of columns of said plurality of partial multi-stage pyramid networks;

routing one or more benchmarks on said programmable integrated circuit;

checking if said one or more benchmarks are successfully routed;

checking if all benchmarks of said one or more benchmarks are successfully routed, then computing a plurality of metrics including area, power, performance of benchmark and routing speed;

checking if all benchmarks of said one or more benchmarks have met a criteria

and if so, saving said multi-stage based pyramid network, or

checking if said one or more benchmarks are not successfully routed, then

changing one or more of said size of said one or more slices, said size of said one or more rings, said size of said plurality of stages, said size of said one or more switches, said size of said plurality of multiplexers, said number of inputs of each multiplexer of said plurality of multiplexers, said connections of said plurality of inlet links and said plurality of outlet links to said plurality of partial multi-stage pyramid networks, said hop length of each external hop wire of said plurality of external hop wires, said setting up of connections of said plurality of external hop wires between said plurality of partial multi-stage pyramid networks, said setting up of connections of said plurality of internal hop wires between said one or more rings, said setting up of connections of said plurality of internal connections between said plurality of stages of the same ring of said one or more rings, said size of said plurality of rows in said two-dimensional grid, said size of said plurality of columns in said two-dimensional grid.

(Exhibit 11.)

47. QuickLogic does not infringe Claim 1 or any other claims of the '399 Patent and seeks such a declaration to resolve the actual dispute between the parties.

FIFTH CLAIM FOR RELIEF

(Declaratory Judgment That QuickLogic Does Not Infringe The '025 Patent)

48. QuickLogic repeats and realleges each and every allegation contained in paragraphs 1 through 47 of this Complaint as if fully set forth herein.

49. In view of the facts and allegations set forth above, there is an actual, justiciable, substantial, and immediate controversy between QuickLogic and Defendants regarding infringement of the '025 Patent.

50. QuickLogic seeks a declaration that it does not infringe, and has not infringed, any claim of the '025 Patent.

51. The '025 Patent is titled "Fast scheduling and optimization of multi-stage hierarchical networks" and purports to "Significantly optimized multi-stage networks with scheduling methods for faster scheduling of connections, useful in wide target applications, with VLSI layouts using only horizontal and vertical links to route large scale sub-integrated circuit blocks having inlet and outlet links, and laid out in an integrated circuit device in a two-dimensional grid arrangement of blocks are presented. The optimized multi-stage networks in each block employ several slices of rings of stages of switches with inlet and outlet links of sub-integrated circuit blocks connecting to rings from either left-hand side only, or from right-hand side only, or from both left-hand side and right-hand side; and employ multi-drop links where outlet links of cross links from switches in a stage of a ring in one sub-integrated circuit block are connected to either inlet links of switches in the another stage of a ring in the same or another sub-integrated circuit block." (Exhibit 12.)

52. Although Defendants have not called out any particular claims as being infringed, Claim 1 of the '025 Patent is exemplary:

> 1. A programmable integrated circuit comprising a plurality of programmable logic blocks and a network,
>
> each programmable logic block of said plurality of programmable logic blocks comprising a plurality of inlet links and a plurality of outlet links; and
>
> said network comprising a plurality of partial multi-stage networks wherein each programmable logic block of said plurality of programmable logic blocks is coupled with at least one of said plurality of partial multi-stage networks; and
>
> said plurality of programmable logic blocks coupled with said plurality of partial multi-stage networks arranged in a two-dimensional grid of a plurality of rows and a plurality of columns; and
>
> each partial multi-stage network of said plurality of partial multi-stage networks further comprising one or more slices, each slice of said one or more slices further comprising one or more rings, each ring of said one or more rings

further comprising y stages, where y≥1; and

each stage of said y stages comprising at least one switch of size $d_i \times d_0$, where $d_i \geq 2$ and $d_0 \geq 2$ and each switch of said at least one switch of size di×d0having di incoming links and d_0 outgoing links; and each switch of said at least one switch of size $d_i \times d_0$ further comprising a plurality of multiplexers of size d≥2 with each multiplexer of said plurality of multiplexers comprising d inputs and one output; and

said at least one switch of size $d_i \times d_0$ comprises either only a forward switch, or only a backward switch, or both a forward switch and a backward switch, or a forward switch, a backward switch and U-turn switch, or a forward switch, a backward switch and a U-turn switch without 180 degree turn paths or a forward switch, a backward switch, a U-turn switch and a reverse U-turn switch or a forward switch, a backward switch, a U-turn switch and a reverse U-turn switch without 180 degree turn paths, or an integrated switch of a forward switch, a backward switch and U-turn switch, or an integrated switch of a forward switch, a backward switch and a U-turn switch without 180 degree turn paths or an integrated switch of a forward switch, a backward switch, a U-turn switch and a reverse U-turn switch or an integrated switch of a forward switch, a backward switch, a U-turn switch and a reverse U-turn switch without 180 degree turn paths; and

said di incoming links and said d0 outgoing links comprises a plurality of internal connections and a plurality of hop wires; and said plurality of hop wires further comprising a plurality of internal hop wires or a plurality of external hop wires; and

each inlet link of said plurality of inlet links is connected to the output of one of said plurality of multiplexers of one switch of said at least one switch of size $d_i \times d_0$ of one stage of said y stages of one partial multi-stage network of said plurality of partial multi-stage networks, and each outlet link of said

plurality of outlet links is connected to one of the inputs of one or more of said plurality of multiplexers of one or more said switches of said at least one switch of size $d_i \times d_0$ of one or more said stages of said y stages of one or more said plurality of partial multi-stage networks; and

a first programmable logic block of said plurality of programmable logic blocks comprising the same or different number of said plurality of inlet links as a second programmable logic block of said plurality of programmable logic blocks and a first programmable logic block of said plurality of programmable logic blocks comprising the same or different number of said plurality of outlet links as a second programmable logic block of said plurality of programmable logic blocks; a first partial multi-stage network of said plurality of partial multi-stage networks comprising the same or different number of said one or more slices as a second partial multi-stage network of said plurality of partial multi-stage networks; a first slice of said one or more slices comprising the same or different number of said one or more rings as a second slice of said one or more slices; a first ring of said one or more rings comprising the same or different number of said y stages as a second ring of said one or more rings; and a first stage of said y stages comprising the same or different number of said at least one switch of size $d_i \times d_0$ as a second stage of said y stages; a first switch of said at least one switch of size $d_i \times d_0$ is the same or different size as a second switch of said at least one switch of size $d_i \times d_0$ a first multiplexer in said plurality of multiplexers of size $d \geq 2$ is the same or different size as a second multiplexer in said plurality of multiplexers of size $d \geq 2$; and

each internal connection of said plurality of internal connections connected from the output of a first multiplexer of said plurality of multiplexers of a first switch of said at least one switch of size $d_i \times d_0$ of a first stage of said y stages of a first ring of said one or more rings to a first input of said d inputs

of a second multiplexer of said plurality of multiplexers of a second switch of said at least one switch of size $d_i \times d_0$ of a second stage of said y stages of the first ring of said one or more rings; and

each internal hop wire of said plurality of internal hop wires is connected from the output of a multiplexer of said plurality of multiplexers of a switch of said at least one switch of size $d_i \times d_0$ of a stage of said y stages of a first ring of said one or more rings of a slice of said one or more slices a first input of said d inputs of one or more multiplexers of said plurality of multiplexers of one or more switches of said at least one switch of size $d_i \times d_0$ of one or more stages of said y stages of one or more rings different from the first ring of said one or more rings of the same slice of said one or more slices; and

each external hop wire of said plurality of external hop wires is connected from the output a multiplexer of said plurality of multiplexers of a switch of said at least one switch of size $d_i \times d_0$ of a stage of said y stages of a ring of said one or more rings of a slice of said one or more slices of a first partial multi-stage network of said plurality of partial multi-stage networks to an input of said d inputs of one or more multiplexers of said plurality of multiplexers of one or more switches of said at least one switch of size $d_i \times d_0$ of one or more stages of said y stages of said one or more rings of a slice of said one or more slices of one or more partial multi-stage networks different from the first partial multi-stage network of said plurality of partial multi-stage networks; and

one or more external hop wires of said plurality of external hop wires are either connected between multiplexers of said plurality of multiplexers of switches of said at least one switch of size $d_i \times d_0$ in same numbered stages of said y stages in two or more partial multi-stage networks of said plurality of partial multi-stage networks or connected between multiplexers of said plurality of multiplexers of switches of said at least one switch of size $d_i \times d_0$ in different

numbered stages of said y stages , when y≥2, in two or more partial multi-stage networks of said plurality of partial multi-stage networks.

(Exhibit 12.)

53. QuickLogic does not infringe Claim 1 or any other claims of the '025 Patent and seeks such a declaration to resolve the actual dispute between the parties.

SIXTH CLAIM FOR RELIEF

(Declaratory Judgment That QuickLogic Does Not Infringe The '594 Patent)

54. QuickLogic repeats and realleges each and every allegation contained in paragraphs 1 through 53 of this Complaint as if fully set forth herein.

55. In view of the facts and allegations set forth above, there is an actual, justiciable, substantial, and immediate controversy between QuickLogic and Defendants regarding infringement of the '594 Patent.

56. QuickLogic seeks a declaration that it does not infringe, and has not infringed, any claim of the '594 Patent.

57. The '594 Patent is titled "Optimization of multi-stage hierarchical networks for practical routing applications" and purports to "Significantly optimized multi-stage networks, useful in wide target applications, with VLSI layouts using only horizontal and vertical links to route large scale sub-integrated circuit blocks having inlet and outlet links, and laid out in an integrated circuit device in a two-dimensional grid arrangement of blocks are presented. The optimized multi-stage networks in each block employ several rings of stages of switches with inlet and outlet links of sub-integrated circuit blocks connecting to rings from either left-hand side only, or from right-hand side only, or from both left-hand side and right-hand side; and employ shuffle exchange links where outlet links of cross links from switches in a stage of a ring in one sub-integrated circuit block are connected to either inlet links of switches in the another stage of a ring in the same or another sub-integrated circuit block." (Exhibit 13.)

58. Although Defendants have not called out any particular claims as being infringed, Claim 1 of the '594 Patent is exemplary:

1. A network implemented in a non-transitory medium comprising a plurality

of partial multi-stage networks and a plurality of inlet links and a plurality of outlet links

said plurality of partial multi-stage networks arranged in a two-dimensional grid of one or more rows and one or more columns; and

each partial multi-stage network of said plurality of partial multi-stage networks comprising a ring and said ring comprising a plurality of stages; and

each stage of said plurality of stages comprising a plurality of switches of size $d_i \times d_0$, where $d_i \geq 2$ and $d_0 \geq 2$ and each switch of said plurality of switches of size $d_i \times d_0$ having di incoming links and d_0 outgoing links; and each switch of said plurality of switches of size $d_i \times d_0$ further comprising a plurality of multiplexers of variable size $d \geq 2$ with each multiplexer of said plurality of multiplexers of variable size $d \geq 2$ comprising d inputs and an output; and

each stage of said plurality of stages comprises either only a forward switch, or only a backward switch, or both a forward switch and a backward switch, or a forward switch, a backward switch and U-turn switch, or a forward switch, a backward switch and a U-turn switch without 180 degree turn paths; and

said d_i incoming links comprises a plurality of internal connections and a plurality of external hop wires, and said d_0 outgoing links comprises a plurality of internal connections and a plurality of external hop wires; and

Each outlet link of Said plurality of outlet links is connected to the output of one multiplexer of said plurality of multiplexers of variable size $d \geq 2$ of one switch of said plurality of switches of size $d_i \times d_0$ of one stage of said plurality of stages of said ring of one partial multi-stage network of said plurality of partial multi-stage networks, and each inlet link of said plurality of inlet links is connected to one input of said d inputs of one or more multiplexers of said plurality of multiplexers of one or more switches of said plurality of switches of one or more stages of said plurality of stages of

said ring of one or more partial multi-stage networks of said plurality of partial multi-stage networks; and

Said ring of a first partial multi-stage network of said plurality of partial multi-stage networks comprising the same or different number of said plurality of stages as said ring of a second partial multi-stage network of said plurality of partial multi-stage networks; a first stage of said plurality of stages comprising the same or different number of said plurality of switches as a second stage of said plurality of stages; a first switch in said plurality of switches of size $d_i \times d_0$ is the same or different size as a second switch in said plurality of switches of size $d_i \times d_0$; a first multiplexer in said plurality of multiplexers of variable size $d \geq 2$ is the same or different size as a second multiplexer in said plurality of multiplexers of variable size $d \geq 2$; and

each internal connection of said plurality of internal connections connected from output of a first multiplexer of said plurality of multiplexers of variable size $d \geq 2$ of said plurality of switches of said ring of a first partial multi-stage network of said plurality of partial multi-stage networks to one input of said d inputs of a second multiplexer of said plurality of multiplexers of variable size $d \geq 2$ of said plurality of switches of said plurality of stages of said ring of said first partial multi-stage network of said plurality of partial multi-stage networks; and

Each external hop wire of said plurality of external hop wires connected from said output of one multiplexer of said plurality of multiplexers of variable size $d \geq 2$ of said plurality of switches of said plurality of stages of said ring of a first partial multi-stage network of said plurality of partial multi-stage networks to one or more inputs of said d inputs of one or more multiplexers of said plurality of multiplexers of said plurality of switches of said plurality of stages of said ring of one or more partial multi-stage networks different from first said partial multi-stage network of said plurality of

partial multi-stage networks; and

one or more external hop wires of said plurality of external hop wires are either connected between said plurality of multiplexers of variable size d≥2 of said plurality of switches of same numbered stages of said plurality of stages of said ring in two or more different partial multi-stage networks of said plurality of partial multi-stage networks or connected between said plurality of multiplexers of variable size d≥2 of said plurality of switches of in different numbered stages said plurality of stages of said ring in two or more partial multi-stage networks of said plurality of partial multi-stage networks.

(Exhibit 13.)

59. QuickLogic does not infringe Claim 1 or any other claims of the '594 Patent and seeks such a declaration to resolve the actual dispute between the parties.

SEVENTH CLAIM FOR RELIEF

(Declaratory Judgment That QuickLogic Does Not Infringe The '597 Patent)

60. QuickLogic repeats and realleges each and every allegation contained in paragraphs 1 through 59 of this Complaint as if fully set forth herein.

61. In view of the facts and allegations set forth above, there is an actual, justiciable, substantial, and immediate controversy between QuickLogic and Defendants regarding infringement of the '597 Patent.

62. QuickLogic seeks a declaration that it does not infringe, and has not infringed, any claim of the '597 Patent.

63. The '597 patent is titled "Fast scheduling and optimization of multi-stage hierarchical networks" and purports to "Significantly optimized multi-stage networks including scheduling methods for faster scheduling of connections, useful in wide target applications, with VLSI layouts using only horizontal wires and vertical wires to route large scale partial multi-stage hierarchical networks having inlet and outlet links, and laid out in an integrated circuit device in a two-dimensional grid arrangement of blocks are disclosed. The optimized multi-stage networks in

each block employ one or more slices of rings of stages of switches with inlet and outlet links of partial multi-stage hierarchical networks connecting to rings from either left-hand side or right-hand side; and employ hop wires or multi-drop hop wires wherein hop wires or multi-drop wires are connected from switches of stages of rings of slices of a first partial multi-stage hierarchical network switches of stages of a rings of slices of the first or a second partial multi-stage hierarchical network." (Exhibit 14.)

64. Although Defendants have not called out any particular claims as being infringed, Claim 1 of the '597 Patent is exemplary:

> 1. A multi-stage hierarchical network comprising:
>
> a plurality of partial multi-stage networks, a plurality of inlet links and a plurality of outlet links, said plurality of partial multi-stage networks arranged in a two-dimensional grid having a plurality of rows and a plurality of columns; and
>
> each partial multi-stage network of said plurality of partial multi-stage networks comprising one or more slices, each slice of said one or more slices comprising one or more rings, each ring of said one or more rings comprising y stages, where $y \geq 2$; and
>
> each stage of said y stages comprising at least one switch of size $d_i \times d_o$, where $d_i \geq 2$ and $d_o \geq 2$, each switch of said at least one switch of size $d_i \times d_o$ having d_i incoming links and do outgoing links, each switch of said at least one switch of size $d_i \times d_o$ comprising a plurality of multiplexers of size $d \geq 2$ with each multiplexer of said plurality of multiplexers comprising d inputs and one output; and
>
> wherein said at least one switch of size $d_i = d_o$ comprises one of a) a forward switch, b) both a forward switch and a U-turn switch, c) a forward switch, a backward switch and a U-turn switch, d) a forward switch, a backward switch, a U-turn switch and a reverse U-turn switch e) a forward switch, a backward switch, a U-turn switch and a reverse U-turn switch without 180-

degree turn paths, and f) an integrated switch comprising a forward switch, a backward switch, a U-turn switch and a reverse U-turn switch without 180-degree turn paths; and

wherein said d_i incoming links and said do outgoing links comprise one or more internal connections and one or more hop wires where said one or more hop wires comprise one or more internal hop wires or one or more external hop wires; and

wherein each outlet link of said plurality of outlet links is connected to the output of a first multiplexer of said plurality of multiplexers of a first switch of said at least one switch of size $d_i \times d_o$ of a first stage of said y stages of a first partial multi-stage network of said plurality of partial multi-stage networks, and each inlet link of said plurality of inlet links is connected to a first input of said d inputs of one or more multiplexers of said plurality of multiplexers of one or more switches of said at least one switch of size $d_i \times d_o$ of one or more stages of said y stages of one or more partial multi-stage networks of said plurality of partial multi-stage networks; and

wherein a first partial multi-stage network of said plurality of partial multi-stage networks comprises one of a) a same number and b) a different number of said plurality of inlet links as a second partial multi-stage network of said plurality of partial multi-stage networks; and a first partial multi-stage of said plurality of partial multi-stage networks comprises one of a) a same number and b) a different number of said plurality of partial multi-stage networks; an first partial multi-stage network of said plurality of partial multi-stage networks; a first partial multi-stage network of said plurality of partial multi-stage networks comprises one of a) a same number and b) a different number of said one or more slices as a second partial multi-stage network of said plurality of partial multi-stage networks; a first slice of said one or more slices comprises one of a) a same number and b) a different

number of said one or more rings as a second slice of said one or more slices; a first ring of said one or more rings comprises one of a) a same number and b) a different number of said y stages as a second ring of said one or more rings; and a first stage of said y stages comprises one of a) a same number and b) a different number of said at least one switch of size $d_i \times d_o$ as a second stage of said y stages; a first switch of said at least one switch of size $d_i \times d_o$ is one of a) a same size and b) a different size as a second switch of said at least one switch of size $d_i \times d_o$; and a first multiplexer in said plurality of multiplexers of size $d \geq 2$ is one of a) a same size and b) a different size as a second size as a second multiplexer in said plurality of multiplexers of size $d \geq 2$; and

wherein each internal connection of said one or more internal connections connected from the output of a first multiplexer of said plurality of multiplexers of a first switch of said at least one switch of size $d_i \times d_o$ of a first stage of said y stages of a first ring of said one or more rings to a first input of said d inputs of a second multiplexer of said plurality of multiplexers of a second switch of said at least one switch of size $d_i \times d_o$ of a second stage of said y stages of the first ring of said one or more rings; and

wherein each internal hop wire of said one or more internal hop wires is connected from the output of a multiplexer of said plurality of multiplexers of a switch of said at least one switch of size $d_i \times d_o$ of a stage of said y stages of a first ring of said one or more rings of a first slice of said one or more slices to a first input of said d inputs of one or more multiplexers of said plurality of multiplexers of one or more switches of said at least one switch of size $d_i \times d_o$ of one or more stages of said y stages of one or more rings different from the first ring of said one or more rings of the first slice of said one or more slices; and

wherein each external hop wire of said one or more external hop wires is

connected from the output a multiplexer of said plurality of multiplexers of a switch of said at least one switch of size $d_i \times d_o$ of a stage of said y stages of a ring of said one or more rings of a slice of said one or more slices of a first partial multi-stage network of said plurality of partial multi-stage networks to an input of said d inputs of one or more multiplexers of said plurality of multiplexers of one or more switches of said at least one switch of size $d_i \times d_o$ of one or more stages of y stages of said one or more rings of a slice of said one or more slices of one or more partial multi-stage networks different from the first partial multi-stage network of said plurality of partial multi-stage networks; and

wherein one or more external hop wires of said one or more external hop wires are one of a) connected between one or more multiplexers of said plurality of multiplexers of one or more switches of said at least one switch of size $d_i \times d_o$ in same stages of said y stages in three or more partial multi-stage networks of said plurality of partial multi-stage networks (hereinafter "multi-drop hop wires") and b) connected between one or more multiplexers of said plurality of multiplexers of one or more switches of said at least one switch of said at least one switch of size $d_i \times d_o$ in different stages of said y stages in three or more partial multi-stage networks of said plurality of partial multi-stage networks (hereinafter "multi-drop hop wires").

(Exhibit 14.)

65. QuickLogic does not infringe Claim 1 or any other claims of the '597 Patent and seeks such a declaration to resolve the actual dispute between the parties.

EIGHTH CLAIM FOR RELIEF

(Declaratory Judgment That QuickLogic Does Not Infringe The '618 Patent)

66. QuickLogic repeats and realleges each and every allegation contained in paragraphs 1 through 65 of this Complaint as if fully set forth herein.

67. In view of the facts and allegations set forth above, there is an actual, justiciable, substantial, and immediate controversy between QuickLogic and Defendants regarding infringement of the ’618 Patent.

68. QuickLogic seeks a declaration that it does not infringe, and has not infringed, any claim of the ’618 Patent.

69. The ’618 patent is titled “Automatic multi-stage fabric generation for FPGAs” and purports to “Systems and methods to automatically or manually generate various multi-stage pyramid network based fabrics, either partially connected or fully connected, are disclosed by changing different parameters of multi-stage pyramid network including such as number of slices, number of rings, number of stages, number of switches, number of multiplexers, the size of the multiplexers in any switch, connections between stages of rings either between the same numbered stages (same level stages) or different numbered stages, single or multi-drop hop wires, hop wires of different hop lengths, hop wires outgoing to different directions, hop wires incoming from different directions, number of hop wires based on the number and type of inlet and outlet links of large scale sub-integrated circuit blocks. One or more parameters are changed in each iteration so that optimized fabrics are generated, at the end of iterations, to route a given set of benchmarks or designs having a specific connection requirements.” (Exhibit 15.)

70. Although Defendants have not called out any particular claims as being infringed, Claim 1 of the ‘618 Patent is exemplary:

> 1 A system for generating a multi-stage pyramid network, said multi-stage pyramid network including connections
>
> to a plurality of computational blocks of a semiconductor integrated circuit arranged in a two-dimensional grid of a plurality of rows and a plurality of columns,
>
> said plurality of computational blocks comprising a plurality of inlet links and a plurality of outlet links; and
>
> said multi-stage pyramid network further comprising a plurality of partial multi-stage pyramid networks wherein each computational block of said plurality

of computational blocks coupled to at least one of said plurality of partial multi-stage pyramid networks via said plurality of inlet links and said plurality of outlet links; and

each partial multi-stage pyramid network of said plurality of partial multi-stage pyramid networks further comprising one or more slices, each slice of said one or more slices further comprising one or more rings, each ring of said one or more rings further comprising a plurality of stages; and

each stage of said plurality of stages comprising one or more switches of size $d_i \times d_0$, where d_i, d_o are integers, $d_i \geq 2$ and $d_o > 2$ and each switch of said one or more switches of size $d_i \times d_0$ having di incoming links and d_0 outgoing links; and each switch of said one or more switches of size $d_i \times d_0$ further comprising a plurality of multiplexers of size $d \geq 2$, where d is an integer, with each multiplexer of said plurality of multiplexers comprising d inputs and one output; and

said one or more switches of size $d_i \times d_0$ comprises either only a forward switch, or only a backward switch, or both a forward switch and a backward switch, or a forward switch, a backward switch and a U-turn switch, or a forward switch, a backward switch and a U-turn switch without 180 degree turn paths or a forward switch, a backward switch, a U-turn switch and a reverse U-turn switch or a forward switch, a backward switch, a U-turn switch and a reverse U-turn switch without 180 degree turn paths, or an integrated switch of a forward switch, a backward switch and a U-turn switch, or an integrated switch of a forward switch, a backward switch and a U-turn switch without 180 degree turn paths or an integrated switch of a forward switch, a backward switch, a U-turn switch and a reverse U-turn switch or an integrated switch of a forward switch, a backward switch, a U-turn switch and a reverse U-turn switch without 180 degree turn paths; and

said di incoming links and said do outgoing links comprises a plurality of

internal connections and a plurality of hop wires; and

each inlet link of said plurality of inlet links is connected to the output of one multiplexer of said plurality of multiplexers of one switch of said one or more switches of one stage of said plurality of stages of one ring of said one or more rings of one slice of said one or more slices of one partial multi-stage pyramid network of said plurality of partial multi-stage pyramid networks, and each outlet link of said plurality of outlet links is connected to an input of said d inputs of one or more multiplexers of said plurality of multiplexers of one or more switches of said one or more switches of one or more stages of said plurality of stages of one or more rings of said one or more rings of one or more slices of said one or more slices of one or more partial multi-stage pyramid networks of said plurality of partial multi-stage pyramid networks; and

a first computational block of said plurality of computational blocks comprising the same or different number of said plurality of inlet links as a second computational block of said plurality of computational blocks; a first computational block of said plurality of computational blocks comprising the same or different number of said plurality of outlet links as a second computational block of said plurality of computational blocks; a first slice of said one or more slices comprising the same or different number of said rings as a second slice of said one or more slices; a first ring of said one or more rings comprising the same or different number of said stages as a second ring of said one or more rings; a first stage of said plurality of stages comprising the same or different number of said switches as a second stage of said plurality of stages; a first switch in said one or more switches is the same or different size as a second switch in said one or more switches; a first multiplexer in said plurality of multiplexers is the same or different size as a second multiplexer in said plurality of multiplexers; and

each internal connection of said plurality of internal connections connected from the output of a first multiplexer of said plurality of multiplexers of a first switch of said one or more switches of a first stage of said plurality of stages of a first ring of said one or more rings to one of the d inputs of a second multiplexer of said plurality of multiplexers of a second switch of said one or more switches of a second stage of said plurality of stages of said first ring of said one or more rings; and

said plurality of hop wires further comprises a plurality of internal hop wires and a plurality of external hop wires; and

each internal hop wire of said plurality of internal hop wires connected from the output of a first multiplexer of said plurality of multiplexers of a first switch of said one or more switches of a first stage of said plurality of stages of a first ring of said one or more rings of a first slice of said one or more slices of a first partial multi-stage pyramid network of said plurality of partial multi-stage pyramid networks to one or more of the d inputs of one or more different multiplexers from said first multiplexer of said plurality of multiplexers of one or more different switches from said first switch of said one or more switches of one or more different stages from said first stage of said plurality of stages of one or more different rings from said first ring of said one or more rings of said first slice of said one or more slices of said first partial multi-stage pyramid network of said plurality of partial multi-stage pyramid networks; and

each external hop wire of said plurality of external hop wires connected from the output of a multiplexer of said plurality of multiplexers of a switch of said one or more switches of a stage of said plurality of stages of a ring of said one or more rings of a slice of said one or more slices of a first said partial multi-stage pyramid network of said plurality of partial multi-stage pyramid networks to one or more inputs of said d inputs of one or more multiplexers

of said plurality of multiplexers of one or more switches of said one or more switches of said plurality of stages of one or more stages of said one or more rings of a slice of said one or more slices of one or more partial multi-stage pyramid networks different from first said partial multi-stage pyramid network of said plurality of partial multi-stage pyramid networks; and

one or more external hop wires of said plurality of external hop wires are either connected between multiplexers of said plurality of multiplexers of switches of said one or more switches of same numbered stages of said plurality of stages in two or more different partial multi-stage pyramid networks of said plurality of partial multi-stage pyramid networks or connected between multiplexers of said plurality of multiplexers of switches of said one or more switches of in different numbered stages said plurality of stages in two or more different partial multi-stage pyramid networks of said plurality of partial multi-stage pyramid networks,

said system comprising:

one or more processors;

a memory arrangement coupled to said one or more processors, the memory arrangement configured with instructions that when executed by said one or more processors cause said one or more processors to perform operations including:

setting up size of said one or more slices, setting up size of said one or more rings, setting up size of said plurality of stages, setting up size of said one or more switches, setting up size of said plurality of multiplexers, setting up number of inputs of each multiplexer of said plurality of multiplexers;

setting up connections of said plurality of inlet links and said plurality of outlet links to said plurality of partial multi-stage pyramid networks;

setting up connections of said plurality of internal connections between said plurality of stages of the same ring of said one or more rings;

selecting hop length of each external hop wire of said plurality of external hop wires setting up connections of said plurality of external hop wires between said plurality of partial multi-stage pyramid networks;

setting up connections of said plurality of internal hop wires between said one or more rings of the same slice of said one or more slices of a partial multi-stage pyramid network of said plurality of partial multi-stage pyramid networks;

setting up size of said plurality of rows and size of said plurality of columns in said two-dimensional grid;

simulating said semiconductor integrated circuit with said plurality of rows and said plurality of columns of said plurality of partial multi-stage pyramid networks;

routing one or more benchmarks on said semiconductor integrated circuit;

checking if said one or more benchmarks are successfully routed;

checking if all benchmarks of said one or more benchmarks are successfully routed, then computing a plurality of metrics including area, power, performance of benchmark and routing speed;

checking if all benchmarks of said one or more benchmarks have met a criteria and if so, saving said multi-stage pyramid network, or

checking if said one or more benchmarks are not successfully routed, then changing one or more of said size of said one or more slices, said size of said one or more rings, said size of said plurality of stages, said size of said one or more switches, said size of said plurality of multiplexers, said number of inputs of each multiplexer of said plurality of multiplexers, said connections of said plurality of inlet links and said plurality of outlet links to said plurality of partial multi-stage pyramid networks, said hop length of each external hop wire of said plurality of external hop wires, said setting up of connections of said plurality of external hop wires between said

plurality of partial multi-stage pyramid networks, said setting up of connections of said plurality of internal hop wires between said one or more rings, said setting up of connections of said plurality of internal connections between said plurality of stages of the same ring of said one or more rings, said size of said plurality of rows in said two-dimensional grid, said size of said plurality of columns in said two-dimensional grid.

(Exhibit 15.)

71. QuickLogic does not infringe Claim 1 or any other claims of the '618 Patent and seeks such a declaration to resolve the actual dispute between the parties.

NINETH CLAIM FOR RELIEF

(Declaratory Judgment That QuickLogic Does Not Infringe The '366 Patent)

72. QuickLogic repeats and realleges each and every allegation contained in paragraphs 1 through 71 of this Complaint as if fully set forth herein.

73. In view of the facts and allegations set forth above, there is an actual, justiciable, substantial, and immediate controversy between QuickLogic and Defendants regarding infringement of the '366 Patent.

74. QuickLogic seeks a declaration that it does not infringe, and has not infringed, any claim of the '366 Patent.

75. The '366 Patent is titled "Optimization of multi-stage hierarchical networks for practical routing applications" and purports to "Significantly optimized multi-stage networks, useful in wide target applications, with VLSI layouts using only horizontal and vertical hop wires to route large scale computational blocks having inlet and outlet links, and laid out in an integrated circuit device in a two-dimensional grid arrangement of partial multi-stage hierarchical networks are presented. The optimized multi-stage networks comprising partial multi-stage hierarchical networks employ one or more rings of stages of switches with inlet and outlet links of computational blocks connecting to rings from either left-hand side, or from right-hand side, or from both left-hand side and right-hand side and employ hop wires from outlet links of switches of a first stage of a first ring of a first partial multi-stage hierarchical network are connected to either

inlet links of switches of the first or a second stage of the first or a second ring of the first or a second partial multi-stage hierarchical network." (Exhibit 16.)

76. Although Defendants have not called out any particular claims as being infringed, Claim 1 of the '366 Patent is exemplary:

> 1 A multi-stage hierarchical network implemented in a non-transitory medium, comprising:
>
> a plurality of partial multi-stage hierarchical networks, a plurality of inlet links and a plurality of outlet links, said plurality of partial multi-stage hierarchical networks arranged in a two-dimensional grid having one or more rows and one or more columns; and
>
> wherein each partial multi-stage hierarchical network of said plurality of partial multi-stage hierarchical networks comprises a ring and said ring comprises a plurality of stages, each stage of said plurality of stages comprising one or more switches of size $d_i \times d_0$, where $d_i \geq 2$ and $d_o \geq 2$, each switch of said one or more switches of size $d_i \times d_0$ having di incoming links and d_0 outgoing links, each switch of said one or more switches of size $d_i \times d_0$ comprising a plurality of multiplexers of size $d \geq 2$ with each multiplexer of said plurality of multiplexers of size $d \geq 2$ comprising d inputs and an output; and
>
> wherein said one or more switches of size $d_i \times d_0$ comprises one of a) a forward switch, a backward switch, a U-turn switch and a reverse U-turn switch and b) a forward switch, a backward switch, a U-turn switch and a reverse U-turn switch without 180-degree turn paths; and
>
> wherein said d_i incoming links and said d_0 outgoing links comprise one or more internal connections or one or more external hop wires; and
>
> wherein each outlet link of said plurality of outlet links is connected to the output of a first multiplexer of said plurality of multiplexers of size $d \geq 2$ of a first switch of said one or more switches of size $d_i \times d_0$ of a first stage of said plurality of stages of said ring of a first partial multi-stage hierarchical

network of said plurality of partial multi-stage hierarchical networks, and each inlet link of said plurality of inlet links is connected to a first input of said d inputs of one or more multiplexers of said plurality of multiplexers of one or more switches of said one or more switches of size $d_i \times d_0$ of one or more stages of said plurality of stages of said ring of one or more partial multi-stage hierarchical networks of said plurality of partial multi-stage hierarchical networks; and

wherein each internal connection of said one or more internal connections connected from the output of a first multiplexer of said plurality of multiplexers of size $d \geq 2$ of a first switch of said one or more switches of size $d_i \times d_0$ of a first stage of said plurality of stages of said ring of a first partial multi-stage hierarchical network of said plurality of partial multi-stage hierarchical networks to a first input of said d inputs of a second multiplexer of said plurality of multiplexers of a second switch of said one or more switches of size $d_i \times d_0$ of a second stage of said plurality of stages of said ring of said first partial multi-stage hierarchical network of said plurality of partial multi-stage hierarchical networks; and

wherein each external hop wire of said one or more external hop wires is connected from said output of a first multiplexer of said plurality of multiplexers of size $d \geq 2$ of a first switch of said one or more switches of size $d_i \times d_0$ of a first stage of said plurality of stages of said ring of a first partial multi-stage hierarchical network of said plurality of partial multi-stage hierarchical networks to an input of said d inputs of one or more multiplexers of said plurality of multiplexers of size $d \geq 2$ of one or more switches of said one or more switches of size $d_i \times d_0$ of one or more stages of said plurality of stages of said ring of one or more partial multi-stage hierarchical networks different from the first partial multi-stage hierarchical network of said plurality of partial multi-stage hierarchical networks; and

wherein one or more external hop wires of said one or more external hop wires are one of a) connected between one or more multiplexers of said plurality of multiplexers of size $d \geq 2$ of one or more switches of said one or more switches of size $d_i \times d_0$ in same stages of said plurality of stages in two partial multi-stage hierarchical networks of said plurality of partial multi-stage hierarchical networks and b) connected between one or more multiplexers of said plurality of multiplexers of size $d \geq 2$ of one or more switches of said one or more switches of size $d_i \times d_0$ in different stages of said plurality of stages in two partial multi-stage hierarchical networks of said plurality of partial multi-stage hierarchical networks.

(Exhibit 16.)

77. QuickLogic does not infringe Claim 1 or any other claims of the '366 Patent and seeks such a declaration to resolve the actual dispute between the parties.

TENTH CLAIM FOR RELIEF

(Declaratory Judgment That QuickLogic Did Not Breach the 2010 Agreement)

78. QuickLogic repeats and realleges each and every allegation contained in paragraphs 1 through 77 of this Complaint as if fully set forth herein.

79. In view of the foregoing, there is an actual, justiciable, substantial, and immediate controversy between QuickLogic and Defendants regarding whether QuickLogic breached any obligation of the 2010 Agreement.

80. QuickLogic requests a judicial determination declaring that it has not breached any obligation of the 2010 Agreement. (Exhibit 3.)

PRAYER FOR RELIEF

QuickLogic respectfully requests the following relief:

A. That the Court enter a judgment declaring that QuickLogic has not infringed and does not infringe any claim of the Asserted Patents;

B. That the Court enter a judgment declaring that QuickLogic did not breach the 2010 Agreement;

C. That the Court declare that this case is exceptional under 35 U.S.C. § 285 and award QuickLogic its attorneys' fees, costs, and expenses incurred in this action;

D. That the Court award QuickLogic any and all other relief to which it may show itself to be entitled; and

E. That the Court award QuickLogic any other relief as the Court may deem just, equitable, and proper.

JURY DEMAND

QuickLogic hereby demands a jury trial on all issues and claims so triable.

Dated: June 16, 2021

BAKER BOTTS L.L.P.

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